Electronic Choices

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- With much help from Paul Rubinov - D0, Fermilab.

Electronics choices

- Criteria
  - The electronics should exist or very close to exist.
  - If the electronics does not completely exist there should be support to get it to exist within an instution which is part of the collaboration.
  - This would require some kind of agreement to provide resources to finish the electronics.
  - Important to understand requirements of electronics.
- I'm looking at 2 kinds. (where the 2d can have modifications.)
  - MINOS Near Detector.
  - TriP - D0 RunIIb upgrade electronics for fiber tracker and preshower.

MINOS Near Detector Electronics

- Near detector uses M64.
- PMT gain 0.33 to 1.0×10^6(maximal gain).
- Requirements.
  - Requirement 150 pe, 0.005 - 24 pc range
  - Threshold 0.3 pe, noise 0.05 pe.
  - Digitization Accuracy 5%.
  - 9400 channels Near, 23000 channels Far.
- Claim 6-8 pe with mirror, but can be lower.
- It exists and we can get more of it.
- Hence, it is well tested and we can be pretty sure that it is well understood.
- Based on KTEV QIE - sensitivity lowered - 2.5 fC/count.
- 8 ranges, 8 bit ADC, output 16 bits, max 200 pc.
- Gain of 10^6 - 160 fC/pe - 65 counts/pe.
- Stores charge in 18.8 ns buckets.
- If channel has $< 1/3$ pe in buckets it is zero suppressed.
- They have 1 meter cables from PMT to electronics.
- noise is 5-6fc for a 19 ns bucket .

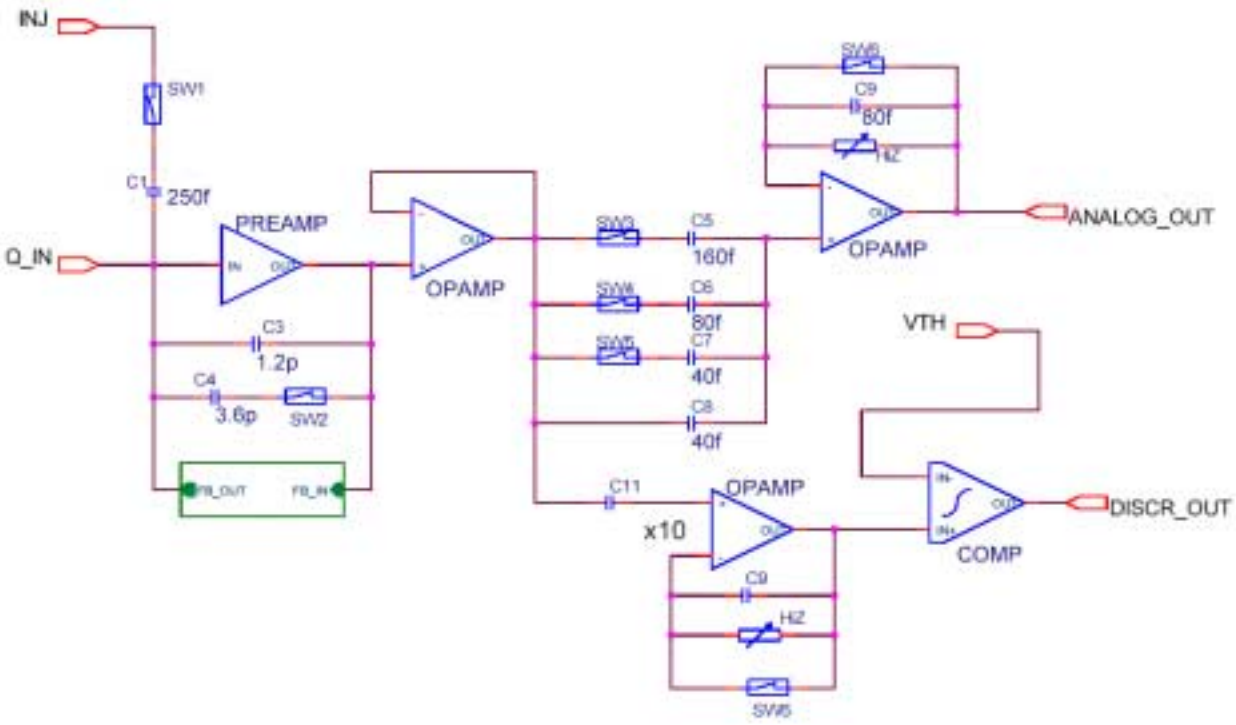
- Unofficial number is \$250-300/channel, MINERvA-\$5M for 20000 channels)
- The electronics does not have timing information. Timing information is gotten by looking at the ratio of charge in different buckets.
  Claim - "couple ns for large pulse height".
  Hence, timing information is not good for particles near MIP.

TriP - D0 Run IIb Fiber Tracker and Shower Max

- D0 has chips for about 200,000 channels of new electronics.
- (These chips will not be used by D0.)
- This electronic is needed for 132 ns bunch crossing, which will not happen.
- The builders are trying to sell it to D0 because of the timing information.
- They are be building 10 prototype boards for $50000.
- Each board reads out 512 channels.
- The builders budgets 500,000 dollars for 100K channels.
- Paul claims costs scales linearly, there are no fixed costs.
- $2500 for a 500 channel board.
  - Later, we will see it is 250 channels for us.
- Could be used for VLCP's or PMTs.

TriP chip

- Made for the collider mode.
- Designed by Abder Mekkaoui with one submission.
- Joint submission with SVX4 prototype run.
- 32 channels/chip.



- Integrator with variable gain.
- Analog_out goes to pipeline 48 buffers deep.
- 2 preamp gains which differ by 4.

- In the design, one can read out 4 of the 48 caps.
  - However, right now it appears that only one of the analogue buffers can be read out.
  - That part of the chip is the same as the SVX4, and they can read out 4 buffers.
  - The chip engineers don't understand why.
  - They will look into it, but its not clear that it will work on the present chip.
- 2 Commercial 12 bit ADCs/TriP chip is used to read out the charge.
- Lowest gain - 5pc max (how we will use the chip).
- Descr_out goes to a latch - 1/2 channels are latched This means chip has equivalent of 16 channels.

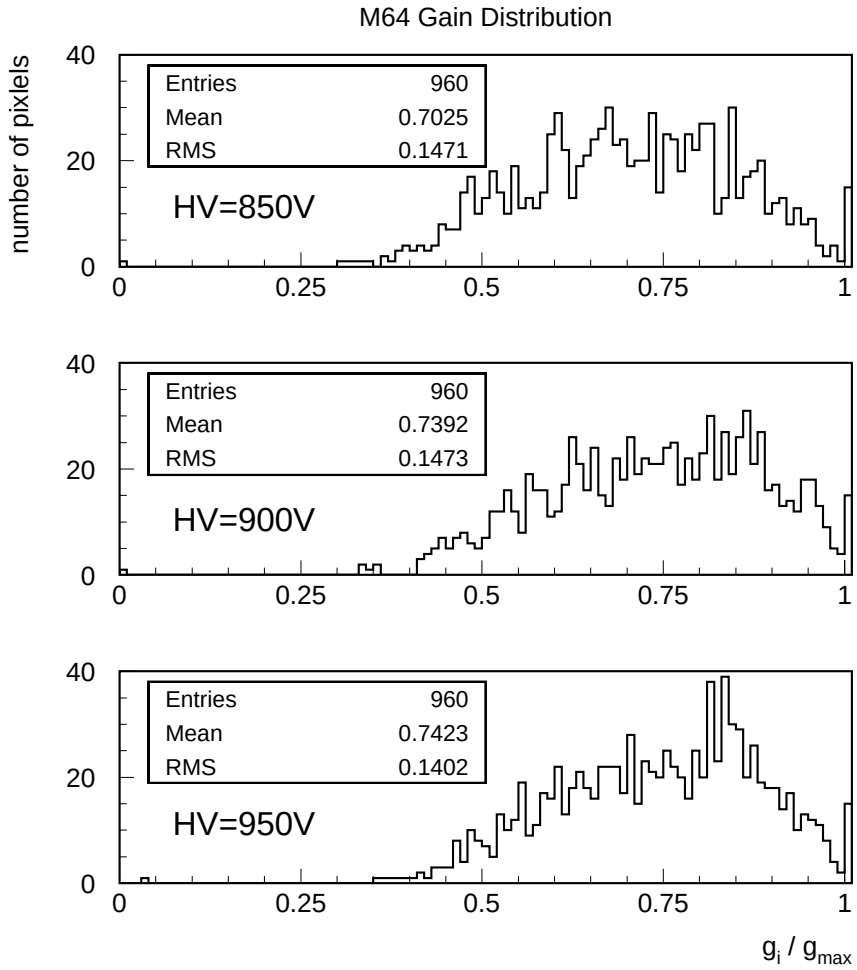
Lets look at ways we could use the chip.

Define how to use chip - closer look later.

- Two Trip Channels per PMT channel with gains differing by a factor of 5
  - Maximal charge = 4pc $\times$ 5 (our diff between low range and high range.)
- This can be done by cap coupling the signal to the 2 channels.
- One gate integrates 10 μ the spill.

Need to understand number of fc for a pe.
Need to understand noise levels.
Need to understand operation of chip compatable with us.

- fc/pe



- The M64 seems to have a gain range of 3.
- We guess that we need to read out 50 mip.
  Its important to understand this number.
  This is bigger than the number MINOS claims.
- For the high gain channel this is 400fC/Mips.
- For the low gain channel this is 125fC/Mips.
- For 8 pe/mip - important to know range of this.
- 15 Fc/pe - gain of 10^5.
- Can increase the gain by increasing the difference between the low and the high range.
- Can put attenuator on from end turn up the gain.

- Noise
  - TriP - 1fC low range, 2 fC high range - for D0
  - But we have a longer gate - for 10μ sec
    2 fC / 10 μs gate with 36 pc cap - high gain .
    4.5 fC / 10 μs gate with 36 pc cap - low gain.
    right now the measurement isn't transparent
    There are external contributions to this.
  - But we have 4-5 m cables (important to keep it short).
  - Lets guess the noise from the cable.
    - CDF cal - 9 fC RMS in B0 with 6 m cable.
      6 fC without cable $\rightarrow$ cable is 6 fC.
      Assuming noise scales with length of cable.
      Charle Nelson claims this is OK to integration time
      5 fC for a 4.5 M cable.
      noise is 6 fC total.
    - CCFR - 60 fc / 250 ns cable. (Mip at 2pc)
      Integration time is 250 ns.
      For 25 ns cable 6 - 8 fC.
    - Total noise say 7 - 8 pC
    - Suggestion - Back terminate the cable in the base.
- 1.5 pe somewhat above the noise, could increase this
- Use 12 bit ADC to readout each trip channel 1fc/count
- look like the range works.

Getting the Timing

- Put output of latch into FPGA.
- Using internal clock of FPGA. get timing so 5 ns.
- Tapped Delay Line can get finer time resolution.
- Latch can be reset with dead time of 15 ns.
- A rough guess as to how will one can get for a mip.
  - D0 gets 3ns sigma for ≥ 8 mips with 3HF, VLPCs, their fiber tracker, and TriP chip.
  - Alan Bross states the decay time for y-11 and 3HF is the same, so maybe equivalent time resolution, slightly bigger.
  - Bicron has fiber with faster dye.
    lose maybe 30% of your light.
- M64 has a dyode out.
  - The can be put into its own special finer grain TDC. Same TDC as for the Timing Scintillator Hodoscope? (Must careful with grounds.)
  - This can give a good timing information for vertex.
  - Not useful for individual tracks.
  - May be helpful for understanding overall timing information.

Gating the ADC

- Gate it for the 10 μ gate.
- There are 48 caps (analogue buffer) on a channel to divide the gate into 48 divisions.
  Takes 15 ns to switch from one cap to another cap.
- The chip was designed to read out 4 of the 48 buffers.
- However, right now, this does not seem to work.
- This part is supposed to be identical to the SVX4 chip, where you can read out multiple buffers.
- Designers do not understand why and will be looking into this.
- But, one may only be able to read out one buffer/channel in this chip.
- Hence, for multiple buffers one need to use the timing information to decide which buffer to read out.
- This could be done after the fact with a "Level 3 Algorithm".
- Or one gets a trigger and readout out this chip and store the ADC value in RAM, maybe 1.6 μ dead, and go live again.

If you can read out more than one buffer

- One could divide 10 μ second spill up into 2.5 μ gates and read out all 4 buffer.
  - One could do reset the amp, 60 ns dead time, or just go to next buffer without resetting amp.
  - If amp is not reset and there is change in both buffers, one must subtract the charge in one buffer from the charge in the preceeding buffers.
    There maybe error if the charge in the preceeding buffers is large or overflows.
- Get trigger, store the charge, and then go to the next buffer with or without a resetting the amp.

Another submission?

- At the very least we like to read out more than one buffer.
- Maybe have individual set threshold.
- Maybe individual control gain.
- Submission by ourselves is about 200K.
- BTEV would like to do a submission.
- In addition D0 would like to do another submission
  - The project would have to be approved.
  - Slow amp down.
  - Need to read out more than one buffer.
  - Want to use Wilkensen converter to get timing to 2 ns in chip, need 6 transistors/channel.
    We would have to look carefully into how we would use this.
- Note that modified chip can be made pin compatable with the old TriP chip.
  Hence, a board design could preceed with the old chip and if a new chip becomes available it could be put on the board.
- In Oct designer available - get chips in May 2003.
- (None of this was discussed with management on 14th floor.)

Is There a Show Stopper?

- The electronics seems to work for us but it would be best if we could get the multiple buffer readout mode to work.
- D0 has done a board layout with this chip and readout of this chip, so that modifying this for us does not seem to be risky.
- We would need a new layout as their layout is setup for VLPCs with boards sticking on top of a cryostat.
- There appears so be no show stopper, especially if the multiple readout works.
- We need to understand noise levels, required maximal mip, and range of photo electrons to really understand this chip and how we might use it.
- How we fit in with the 14th floor would have to be in the proposal. We would need resources.

Costs?

- The present TriP chips reads out 200000 channels (100000 channels - 2 per channel) are free.
  They will not be used.
- D0 estimates 512 channels board (256 channel for us) is $2000
- We would have to determine how many channels go on a board.
  Hence, we might want to understand how the layout of the experiment feeds into the layout of the electronics.
- Cost of another submission, 1 month of chip engineer and whether D0 and BTEV comes along.

For the future?

- Get more detailed understanding in how would things work.
- Setting up with M64 on HV with correct cable lenght on a D0 board.
  Using board which goes from connectors to this flex cable.
  D0 forward detector uses 16 channel pmt.
- Determining resources needed and request them.
- If we decide to go with this option and the proposal is accepted, we would probably want to go fairly quickly building a board.
- The board would have 64 channels, with all the readout capibility we want.
- Cost a couple of thousand dollars and about 3 months of Paul's time.

Conclusion

- MINOS electrons easy, but not good timing information.
- TriP could work and does not look risky
  We could probably figure out it does not work before we become completely committed.
- We would need some resources from the 14th Floor.
- No real show stopper at this point for TriP chip.